Minority Carrier Tunneling and Stress-Induced Leakage Current for p^+ gate MOS Capacitors with Poly-Si and Poly-$Si_{0.7}Ge_{0.3}$ Gate Material

V.E. Houtsma*, J. Holleman*, C. Salm*, I. R. de Haan*,
J. Schmitz†, F. P. Widdershoven† and P.H. Woerlee†*

* MESA Research Institute, University of Twente, P.O.Box 217, 7500AE Enschede, The Netherlands.
† Philips Research Laboratories, Prof. Holstlaan 4, 5656AA Eindhoven, The Netherlands.

Abstract

In this paper the I-V conduction mechanism for gate injection ($-V_g$), Stress-Induced Leakage Current(SILC) characteristics and time-to-breakdown(t_{bd}) of PMOS capacitors with p^+-poly-Si and poly-SiGe gate material on 5.6,4.8 and 3.1 nm oxide thickness are studied. A model based on Minority Carrier Tunneling(MCT) from the gate is proposed for the I-V and SILC characteristics at $-V_g$ of our devices. Time-to-breakdown data are presented and discussed.

Introduction

The integrity of ultra-thin oxides is a major concern for further downscaling of the gate oxide thickness. Stress-Induced Leakage Current(SILC), soft-breakdown(SB) and the increase of temperature acceleration of time-to-breakdown (t_{bd}) limit the downscaling of gate oxide thickness [1,2,3]. Gate oxide reliability has been studied mainly for n^+-doped poly-Si gate devices. The degradation of PMOS gate dielectric is also a major concern. Recently, first reports on the conduction(I-V), SILC and degradation mechanisms in p^+ gate devices were presented [4,5,6]. However a complete understanding is still not available. In this work the I-V conduction mechanism for gate injection, SILC characteristics and reliability of PMOS capacitors with p^+-gate material on 5.6,4.8 and 3.1 nm oxide thickness are studied. P^+-gates with poly-Si and poly-$Si_{0.7}Ge_{0.3}$ are used to study the influence of gate workfunction on gate current and SILC current.

I-V Conduction Mechanism

I-V measurements are performed on gated diode structures for both gate bias polarities. Fig. 1 displays the J-E characteristics of the unstressed p^+ poly-Si and poly-SiGe capacitors(5.6 nm) for substrate and gate injection conditions (n^+ shown as reference). The oxide field was obtained by integration of the high frequency(10 kHz) C-V curve (gated-diode) [6]. The onset of conduction at $-V_g$ occurs at significantly higher oxide field (1.5×) than for $+V_g$ condition. Note the difference between poly-Si and poly-SiGe for $-V_g$. A carrier separation technique was used in [7] to show that electron injection from the gate is dominating the tunnel current. Hole tunneling from the substrate is negligible for thicker oxides (>4 nm) (Fig. 2)

In Fig. 3 the J-E characteristics of PMOS capacitors on 4.8 nm oxide with different RTA gate anneal are shown. It can be observed that for $-V_g$ with increasing RTA temperature the J-E characteristics shift to higher oxide fields.

For very thin oxides (<4 nm) another contribution to the I-V curve at $-V_g$ is observed. Carrier separation measurements show that holes can tunnel from the substrate to the gate ($+I_{s/d}$), see Fig. 4. This current increases strongly with electrical stress, indicating that it is trap related. A possible mechanism could be trap assisted hole tunneling from the substrate (HTAT). Moreover, this current increases strongly with decreasing oxide thickness and can be important for the degradation of ultra-thin oxides, since hot-holes are no longer needed to trigger the breakdown process [8]. Note that this current can be of importance for very thin oxide n^+ gate devices at $-V_g$ condition and as MCT for $+V_g$.
At higher V_{ox}, $I_{s/d}$ changes sign due to impact ionisation of electrons coming from the gate.

I-V Model for Gate Injection

For thick oxides(> 4 nm) there are three possible mechanisms for electron injection from the gate (Fig. 2). The first possibility is valence band tunneling(VBT), however a FN expression with ϕ_b=4.2 eV(poly-Si) can not be used to fit the I-V curves at $-V_g$ (Fig. 3) [4,9]. A second possibility is tunneling of electrons from interface states(IST), which are present at the poly-Si/SiO_2 interface. This current might be important but will be neglected in first approximation to investigate MCT only. A third possibility is tunneling of minority carriers (MCT), i.e. electrons from the conduction band of the gate. A first order model of MCT was developed based on the Esaki-Tsu tunneling formula [10] :

$$J(\phi_B, t_{ox}, E_{ox}) = \frac{n_v m_d k_B T}{2\pi^2 \hbar^3} \int_0^\infty T^* T_{WKB} \cdot \ln(1+\exp(\frac{E_F - E}{k_B T}))dE$$

$$E_F = E_C - E_g + qV_{poly}$$

Note that under FN tunneling the Fermi-level is located at the conduction band edge i.e. E_F=E_C, however for MCT E_F«E_C. The difference in energy between the Fermi level in the gate and the conduction band edge at the SiO_2 interface is gate voltage dependent due to gate depletion. The potential drop over the gate depletion layer V_{poly} is estimated from measured C-V curves.

0-7803-5410-9/99/$10.00 © 1999 IEEE

Calculated J-E characteristics with $N_{poly}=2\cdot10^{19}cm^{-3}$ (poly-Si and poly-SiGe) of MCT agree reasonably well with measurements (Figs. 5 and 6). The difference between poly-Si and poly-SiGe is related to a decrease in bandgap E_g for MCT. This indicates that MCT is important for the gate doping used in our devices. Refining the MCT model also requires inclusion of non-uniform injection (doping level varies over grain) and the limited generation of carriers available for tunneling. The latter effect is also observed from C-V measurements, see Fig. 7. High frequency(10 kHz) C-V curves on 4.8 nm oxide thickness show no sharp onset of inversion as is observed in n^+ gate devices [11], hence carrier tunneling out of the gate occurs at a higher rate than that of carrier generation. This indicates that V_{poly} which is an important parameter for MCT, can be determined with limited accuracy only. The dependence of the J-E characteristics at $-V_g$ on gate anneal RTA temperature (Fig. 3) is also explained using MCT. Gate doping at the SiO_2 interface increases with increasing RTA temperature and a higher oxide field is needed to obtain the same tunnel current.

So for gate injection conditions, a significantly larger oxide field is required to obtain the same tunneling current as for substrate injection conditions. This will also influence the SILC characteristics. Results are discussed below.

SILC Characteristics

Electrical stress has been applied on $A=4.0\cdot10^{-4}$ cm^{-2} poly-Si and poly-SiGe PMOS capacitors on 5.6 nm oxide thickness using constant current stress(CCS) conditions of $J_{stress}=\pm0.1$ mA/cm^2. SILC was measured in a similar way as in [2]. In Figs. 8 and 9 the J-E characteristics of p^+ poly-Si and poly-SiGe gate devices are shown after various stress intervals. For $-V_g$ injection SILC becomes apparent at much higher oxide fields compared to $+V_g$. Furthermore the field dependence is different from that at $+V_g$. At comparable oxide field SILC is orders of magnitude smaller for $-V_g$ stress than for $+V_g$ stress. This is different from n^+-poly gate devices where SILC is almost symmetric with gate polarity [2]. The reduced SILC for poly-SiGe compared to poly-Si could be a result of reduced boron incorporation in the gate oxide or a lower oxide field at the same stress current (CCS).

SILC is assumed to be due to trap-assisted tunneling(TAT) and it is observed that SILC is proportional to the neutral trap density created during stress [12]. Fig. 10 shows the gate and source/drain current of p^+ poly-Si gate MOSFETs on 4.8 nm gate oxide thickness before and after $-V_g$ stressing. Note that after stressing an increase of source/drain current ($+I_{s/d}$) is observed which flows from the source/drain to the gate and is most likely due to HTAT. The quantum yield (corrected for HTAT) before and after $-V_g$ stressing is given in Fig. 11. It can be observed that the electrons in the SILC process after $-V_g$ stress lose an energy of 1.0 eV, which is slightly lower as observed for n^+ gate devices [10]. This difference could be related to a thinner oxide thickness in this case.

A model based on *inelastic* TAT was developed similar to that in [10] to model the SILC current under FN, MCT and VBT injection conditions. The hole current (HTAT) is not included in the model, since it is negligible for $t_{ox}=5.6$ nm. The cross section of the traps is taken from [13] to be $\sigma=1\cdot10^{-15}$ cm^2, however significant only as far as orders of magnitude are concerned. E_{relax} is assumed to be 1.5 eV for $t_{ox}=5.6$ nm.

The $+V_g$ SILC after $+V_g$ stress can be described well under FN injection assuming a neutral trap volume density of $N_{trap}=9.2\cdot10^{17}$ cm^{-3} (Fig. 12). For $-V_g$ stress the SILC current at $-V_g$ is caused by TAT of valence band electrons for E<7 MV/cm ($N_{trap}=5.6\cdot10^{18}$ cm^{-3}), since gate depletion is reduced. For high oxide fields TAT of conduction band electrons is the dominant conduction mechanism with $N_{trap}=1.1\cdot10^{19}$ cm^{-3} (Fig. 13). This increase of neutral traps for $-V_g$ stress (10×) is most likely due to the higher oxide field at $-V_g$ during stress at the same current (CCS). This is confirmed by Figs. 14 and 15 were the SILC characteristics are measured for $+V_g$ and $-V_g$ after opposite stress bias polarity conditions. For $+V_g$ also an increase of SILC is observed (10×), while at $-V_g$ SILC is significantly reduced.

Time-to-breakdown Measurements

Time-to-breakdown(t_{bd}) data of ultra-thin gate oxides with p^+ gates on 4.8 nm gate oxides under constant voltage stress (CVS) conditions of $V_g=-6.5$ V are shown in Fig. 16. An increase of t_{bd} with increasing gate anneal RTA temperature is observed, which is most likely related to a decrease in tunneling current during stress at a fixed gate voltage. This shows that not only V_g but also the electron fluence J_{stress} are important parameters for t_{bd}.

Conclusions

For p^+ gate devices three mechanisms (VBT, IST and MCT) were proposed for the conduction mechanism under gate injection conditions ($-V_g$). MCT seems to be an important conduction mechanism at $-V_g$ for realistic doping concentrations used in our devices. For thin oxides(<4 nm), a hole current from substrate to gate is observed, becoming increasingly important with decreasing oxide thickness. The gate anneal RTA temperature strongly influences the time-to-breakdown for p^+ gate devices under CVS conditions.

References

[1] D. J. Maria et al., Apl. Phys. Lett. Vol 74 1999 pp 1752
[2] J. De Blauwe et al., IEDM Tech. Digest, 1996 pp 343
[3] J. H. Stathis et al., IEDM Tech. Digest, 1998 pp 167
[4] C. Salm et al., Electron Dev. Lett. Vol 19 1998 pp 213
[5] Y. Shi et al., Electron Dev. Lett. Vol 19 1998 pp 391
[6] V.E. Houtsma et al., Electron Dev. Lett. Vol 20 1999 pp 314
[7] V.E. Houtsma et al., Microelec. Eng. (INFOS'99) in press.
[8] K. Schuegraf et al., Int. Rel. Phys. Sym. Proc. 93, 1993 pp7
[9] J. -L. Ogier et al., Proc. ESSDERC96, 1996 pp763
[10] S. Takagi et al., Trans. Elec. Dev. Vol 46 1999 pp 348
[11] C.-Y. Lu et al., Electron Dev. Lett. Vol 10 1989 pp 192
[12] D. J. Dimaria et al., J. Appl. Phys. Vol 78 1995 pp 38
[13] K. Sakakibara et al., Trans. Elec. Dev. Vol 44 1997 pp 1002

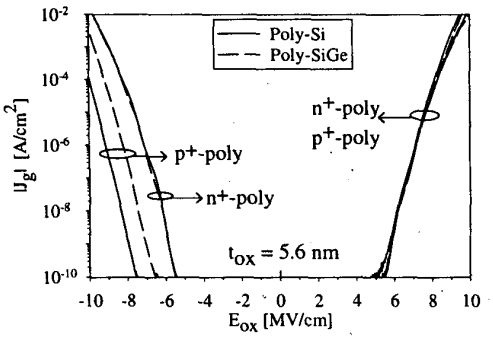

Fig. 1: J-E measurements of unstressed poly-Si and poly-SiGe gate MOS capacitors. Dashed line poly-SiGe, solid line poly-Si.

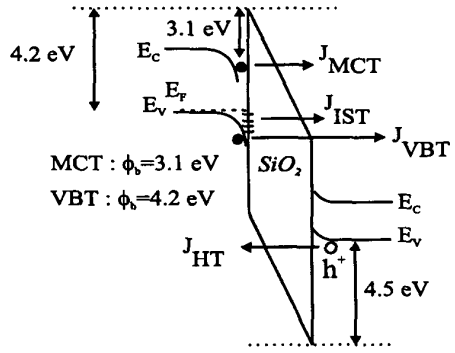

Fig. 2: Schematic representation of the four possible tunneling mechanisms for p^+ gate devices under $-V_g$ bias condition.

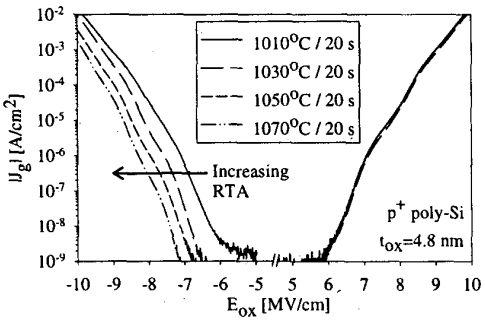

Fig. 3: J-E characteristics of p^+ poly-Si gate devices on 4.8 nm gate oxide. The gate anneal RTA temperature is varied from 1010°C to 1070°C.

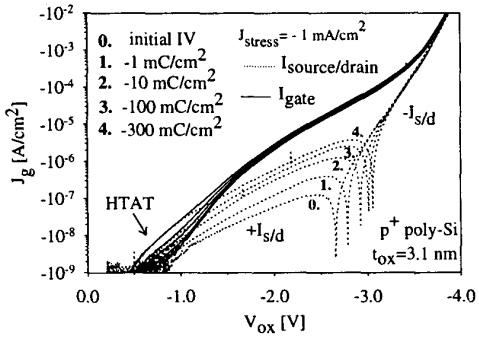

Fig. 4: Carrier separation measurements on p^+ gate devices (3.1 nm). A large increase of hole current is observed with increasing electrical stress.

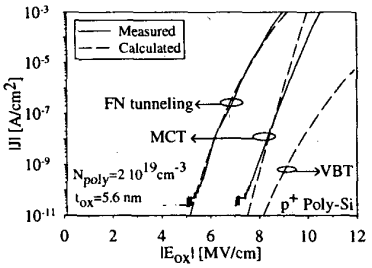

Fig. 5: Calculated and measured J-E characteristics for p^+ poly-Si gate devices on 5.6 nm gate oxides.

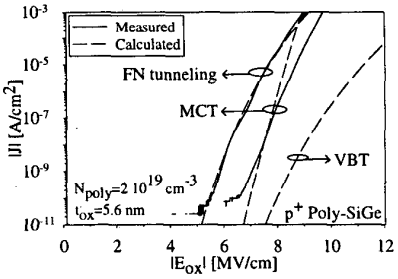

Fig. 6: Calculated and measured J-E characteristics for p^+ poly-SiGe gate devices on 5.6 nm gate oxides.

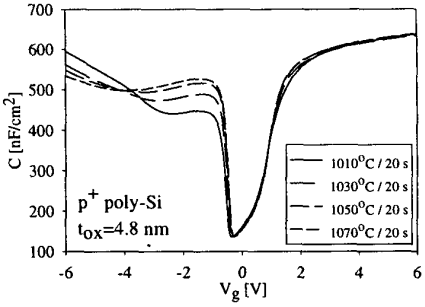

Fig. 7: High freq. C-V characteristics (gated-diode) of p^+ poly-Si gate devices on 4.8 nm gate oxide. The gate anneal RTA temperature is varied from 1010°C to 1070°C

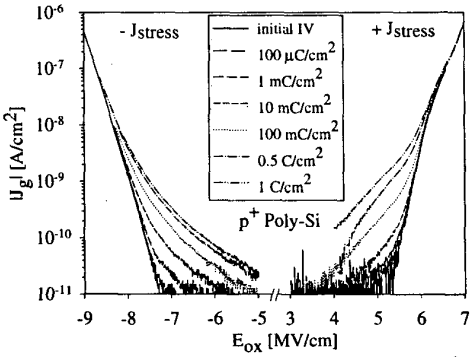

Fig. 8: Measured J-E curves before and after stress (100μC/cm^2 to 1C/cm^2) for p^+ poly-Si gate material on 5.6 nm gate oxide thickness.

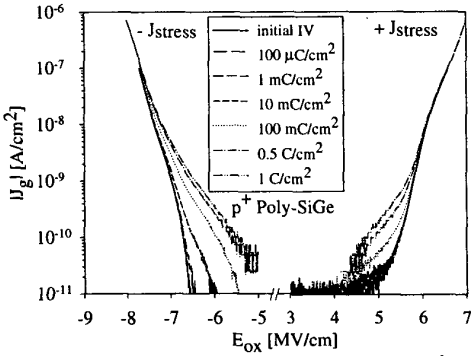

Fig. 9: Measured J-E curves before and after stress (100μC/cm^2 to 1C/cm^2) for p^+ poly-SiGe gate material on 5.6 nm gate oxide thickness.

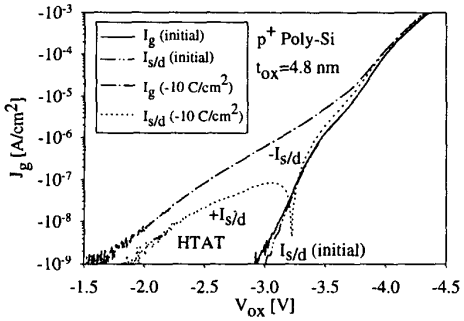

Fig 10: Gate and source/drain currents of PMOSFETs on 4.8 nm gate oxides before and after MCT stressing.

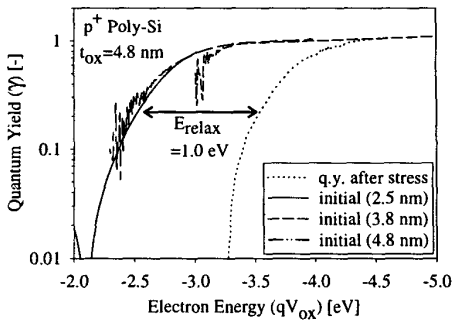

Fig. 11: Measured quantum yield of p$^+$ gate devices before and after MCT stressing. An energy loss of E_{relax}=1.0 eV is clearly observed.

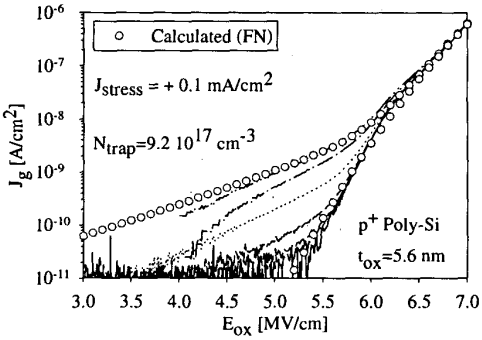

Fig. 12: Calculated and measured SILC at +V_g for p$^+$ poly-Si gate devices on 5.6 nm gate oxide thickness (see Fig. 8).

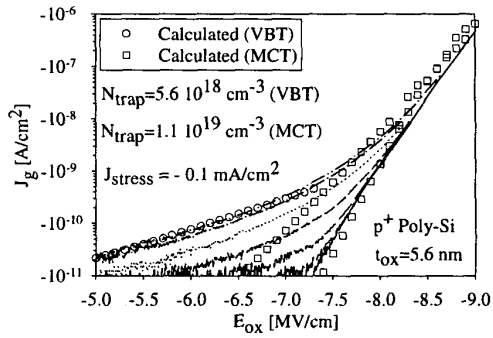

Fig. 13: Calculated and measured SILC at -V_g for p$^+$ poly-Si gate devices on 5.6 nm gate oxide thickness (see Fig. 8).

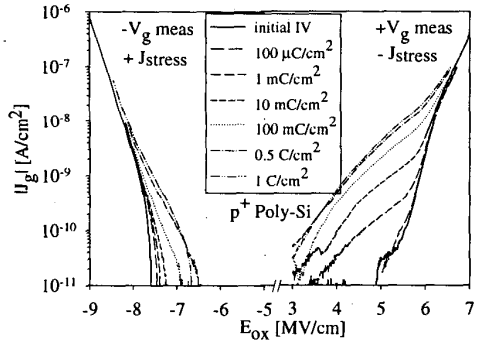

Fig. 14: Measured J-E curves before and after stress for p$^+$ poly-Si gate material (5.6 nm). Stressing takes place under opposite gate bias polarity.

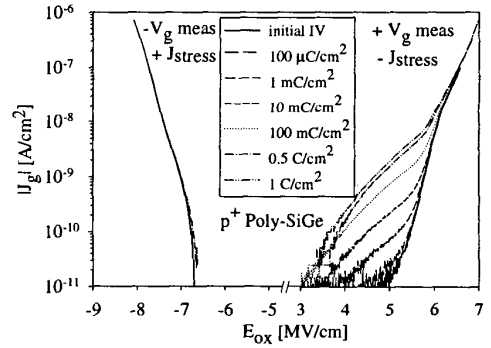

Fig. 15: Measured J-E curves before and after stress for p$^+$ poly-SiGe gate material (5.6 nm). Stressing takes place under opposite gate bias polarity.

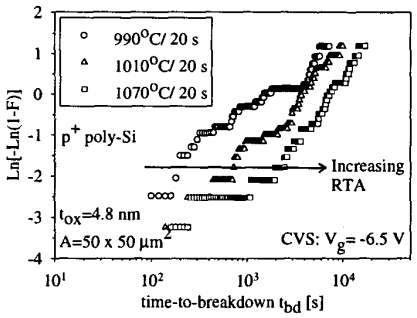

Fig. 16: t_{bd} measurements on p$^+$ poly-Si gates on 4.8 nm gate oxides at V_g=-6.5 V. The gate anneal RTA temperature is 990°C, 1070°C and 1070°C.